Applicant: Yoshinori Hino et al.

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Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

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Listing of Claims:

- 1. (Currently Amended) A semiconductor device comprising:
- a plurality of regions representing output bits; and
- a dummy pattern having the same shape as the output bits formed to be adjacent to the end portion of a output bit group, wherein each output bit group constituting a cathode driver, an anode driver and an anode driver for icon.
 - 2. (Currently Amended) A semiconductor device for a driver comprising:
 - a plurality of output one bits constituting an output bit group; and
- a dummy pattern having the same shape as the output bits formed to be adjacent to the end portion of the output bit group, wherein each output bit group constituting a cathode driver, an anode driver and an anode driver for icon.
- 3. (Original) The semiconductor device according to claim 2, wherein the dummy pattern is formed at an empty space in a region where a plurality of output bits are arranged.
- 4. (Canceled) The semiconductor device according to claim 2, wherein the dummy pattern is formed to be adjacent to the end portion of each output bit group constituting a cathode driver, an anode driver and an anode driver for icon.
- 5. (Currently Amended) The semiconductor device according to claim [4] 2, wherein number of outputs of the dummy pattern formed at a region where output bit groups constituting the cathode driver, the anode driver and the anode driver for icon are adjacent each other is less

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than number of outputs of the dummy pattern formed at a region where output bit groups are not adjacent each other.

6. (Original) The semiconductor device according to claim 2, wherein the dummy pattern has the same shape as a wiring for gate electrode.

7. (Currently Amended) A pattern layout method of a semiconductor device arranged with plural output bits comprising:

forming a dummy pattern having the same shape as the output bits to be adjacent to an end portion of an output bit group, wherein each output bit group constituting a cathode driver, an anode driver and an anode driver for icon.

8. (Currently Amended) A pattern layout method of a semiconductor device arranged with plural output one bits and constituting an output bit group comprising:

forming a dummy pattern having the same shape as the output bits to be adjacent to an end portion of the output bit group, wherein each output bit group constituting a cathode driver, an anode driver and an anode driver for icon.

- 9. (Original) The pattern layout method of a semiconductor according to claim 8, wherein the dummy pattern is formed at an empty space in a region where the plural output bits are arranged.
- 10. (Canceled) The pattern layout method of a semiconductor according to claim 8, wherein the dummy pattern is formed to be adjacent to the end portion of each output bit group constituting a cathode driver, an anode driver, and an anode driver for icon.
- 11. (Currently Amended) The pattern layout method of a semiconductor according to claim 10 8, wherein number of outputs of the dummy pattern formed at a region where output bit

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groups constituting the cathode driver, the anode driver, and the anode driver for icon are adjacent each other is less than number of outputs of the dummy pattern formed at a region where output bit groups are not adjacent each other.

12. (Original) The pattern layout method of a semiconductor according to claim 8, wherein the dummy pattern has the same shape as a wiring for gate electrode.